B.E. Fifth Semester (Computer Engineering) (C.B.S.)

Computer Architecture & Organization

P. Pages : 2 **NKT/KS/17/7361**

Time : Three Hours * 0 0 6 0 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Assume suitable data whenever necessary.
9. Illustrate your answers whenever necessary with the help of neat sketches.
10. Use of non programmable calculator is permitted.

1. a) Draw and Explain The Von Neumann Machine. Architecture. **7**

b) What is Bus Interconnection and Explain peripheral component Interconnect (PCI) configuration. **6**

OR

2. a) Explain Booth Multiplication algorithm with an example. **7**

b) Explain floating-point Representation with an example. **6**

3. a) What do you mean by Addressing Modes? Discuss the various addressing Modes of a general purpose processor with example. **8**

b) What is pipelining?
Give examples of pipelining. **6**

OR

4. a) Explain the Data flow for fetch cycle and Indirect cycle in Instruction cycle. **7**

b) Explain ALU organization with neat sketch. **7**

5. a) Explain hardwired control unit. Why it is called hardwired? **6**

b) Explain control sequence for $\text{Sub}(r_1), r_2$ By using two bus organization. **7**

OR

6. a) Explain the Wilkes Micro-programmed control unit. **8**

b) Explain vertical and Horizontal Micro Instruction. **5**

7.	a)	Draw and Explain structure of Dynamic RAM cell and compare with static RAM cell.	**7**
	b)	Describe Virtual Memory system and explain the concept of locality of Reference.	**6**

OR

8.	a)	Consider a cache consisting of 128 blocks of 16 words each to form 2k words. Main Memory has 4k blocks of 16 words in each block to form a 64k words. Find out the number of bits required for TAG, BLOCK, WORD for :- i) Direct Mapped cache ii) Associative Mapped iii) Set Associative Mapped cache with two blocks per set.	**8**
	b)	Explain various Types of Read-Only-Memories (ROM)	**5**
9.	a)	What is DNA? Explain DNA and Interrupt breakpoints during an Instruction cycle.	**7**
	b)	Explain Asynchronous Transmission and synchronous Transmission.	**7**

OR

10.		Explain the following Interface circuits with neat sketch i) Parallel port ii) Serial port	**14**
11.	a)	Explain cluster configurations with neat diagram.	**7**
	b)	Compare RISC and CISC processor.	**3**
	c)	Write types of parallel processor systems.	**3**

OR

12.	a)	Draw and explain the structure for a symmetric multiprocessor.	**7**
	b)	Explain the approaches to vector computation.	**6**

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